

FIG. 1

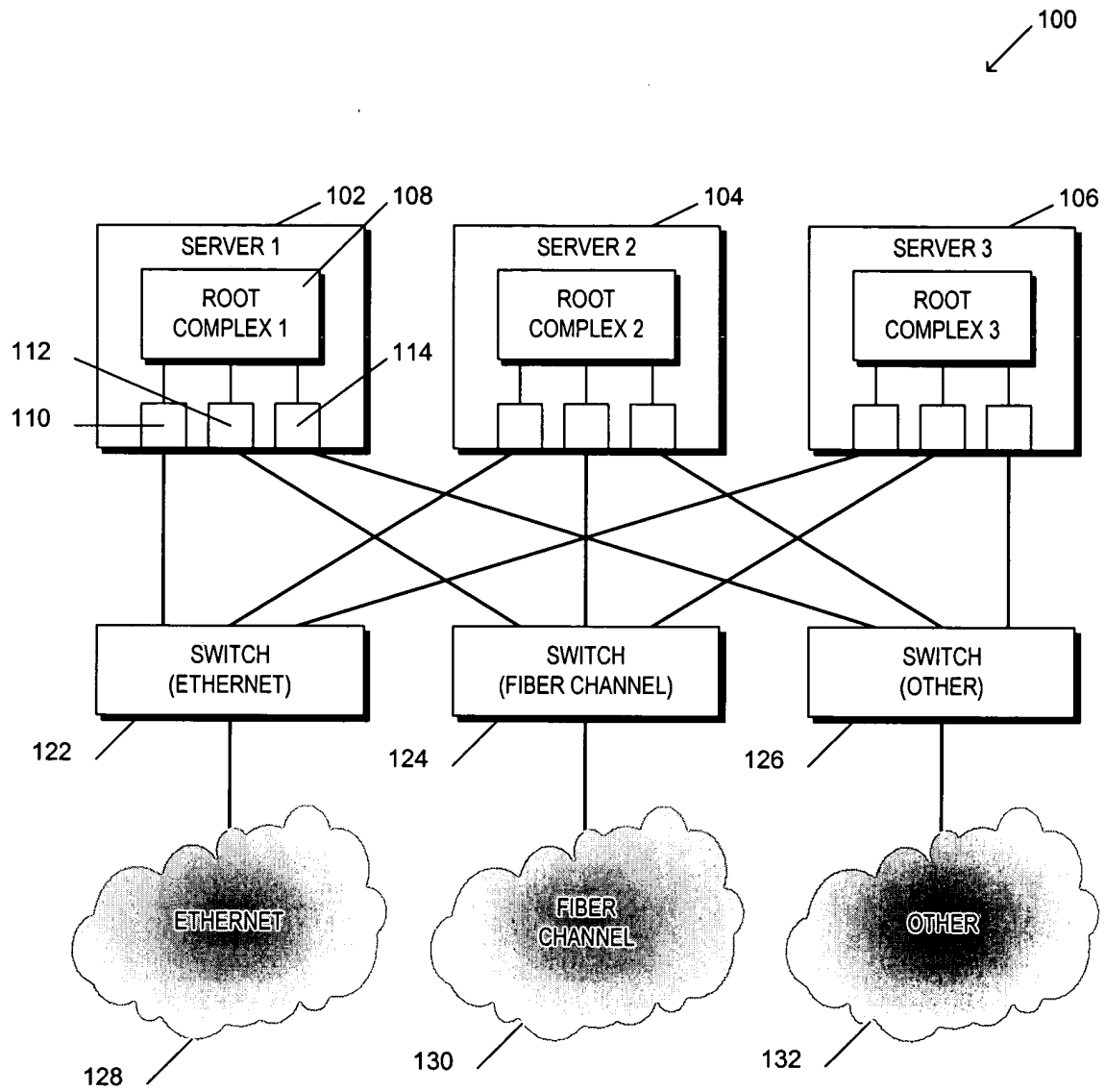


FIG. 2A

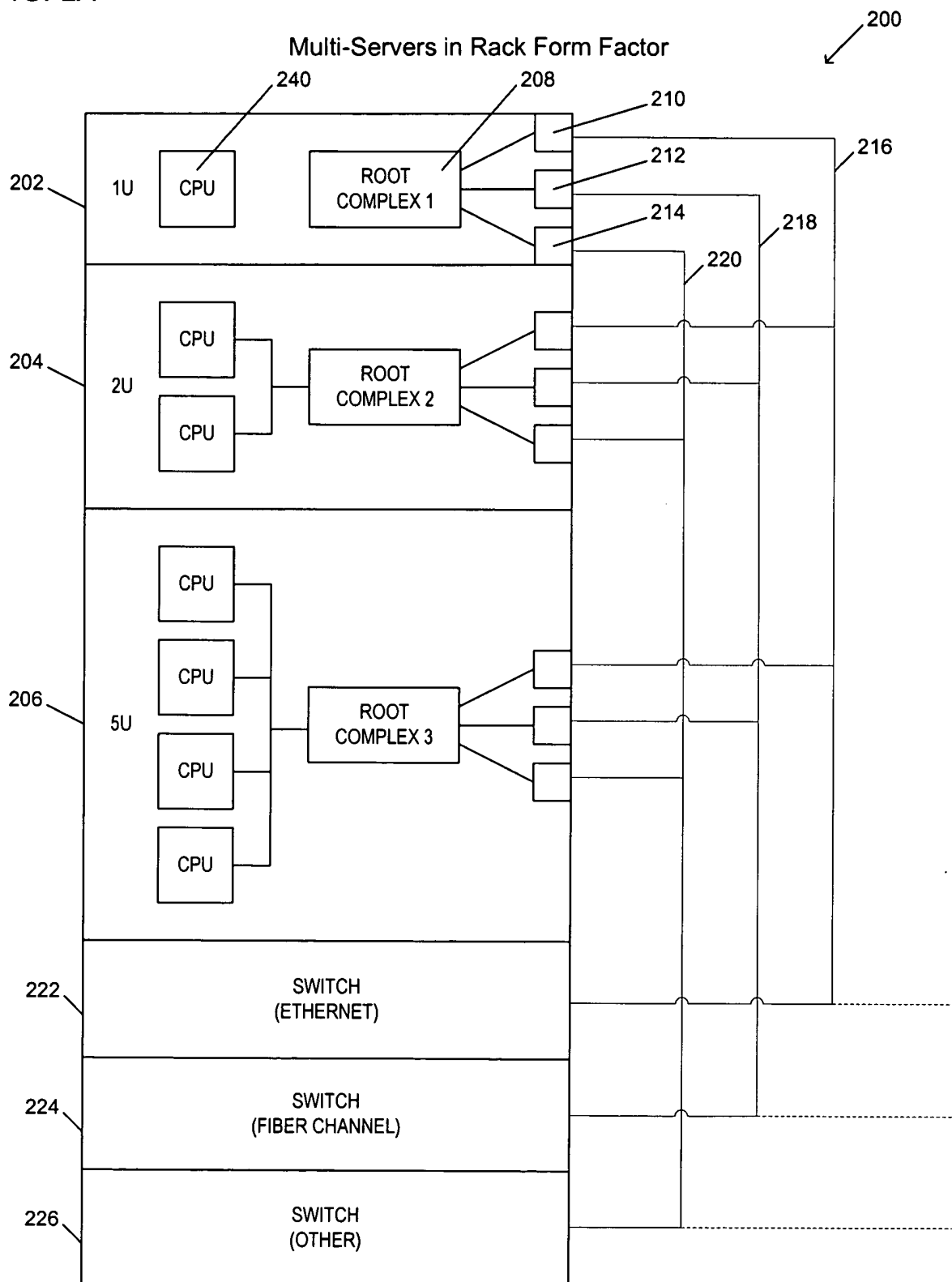


FIG. 2B

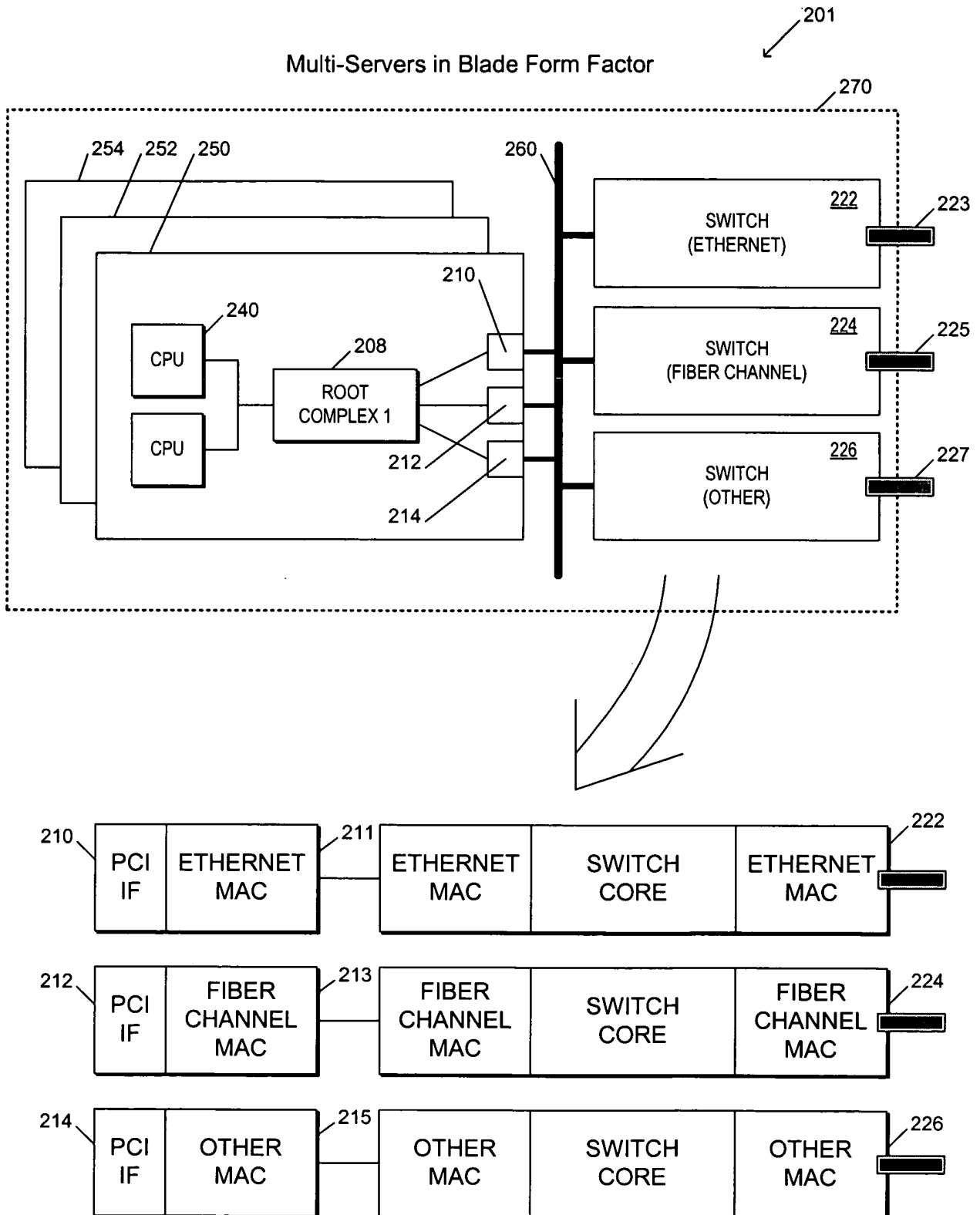


FIG. 2C

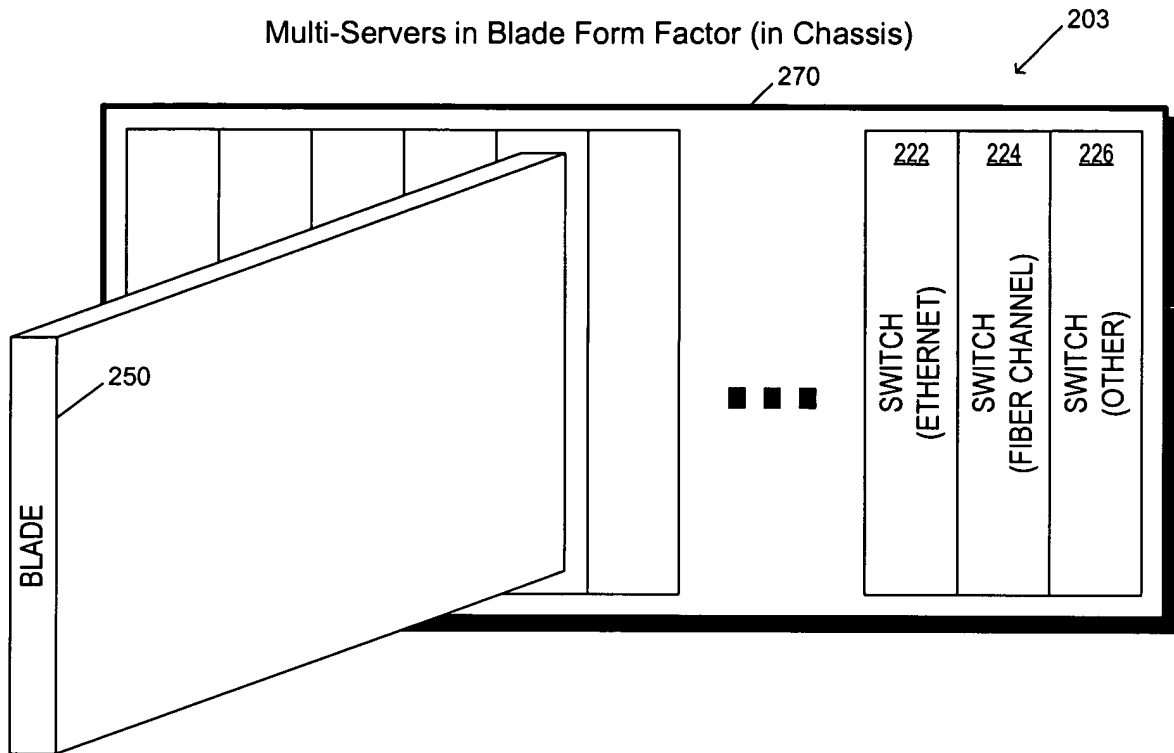


FIG. 3

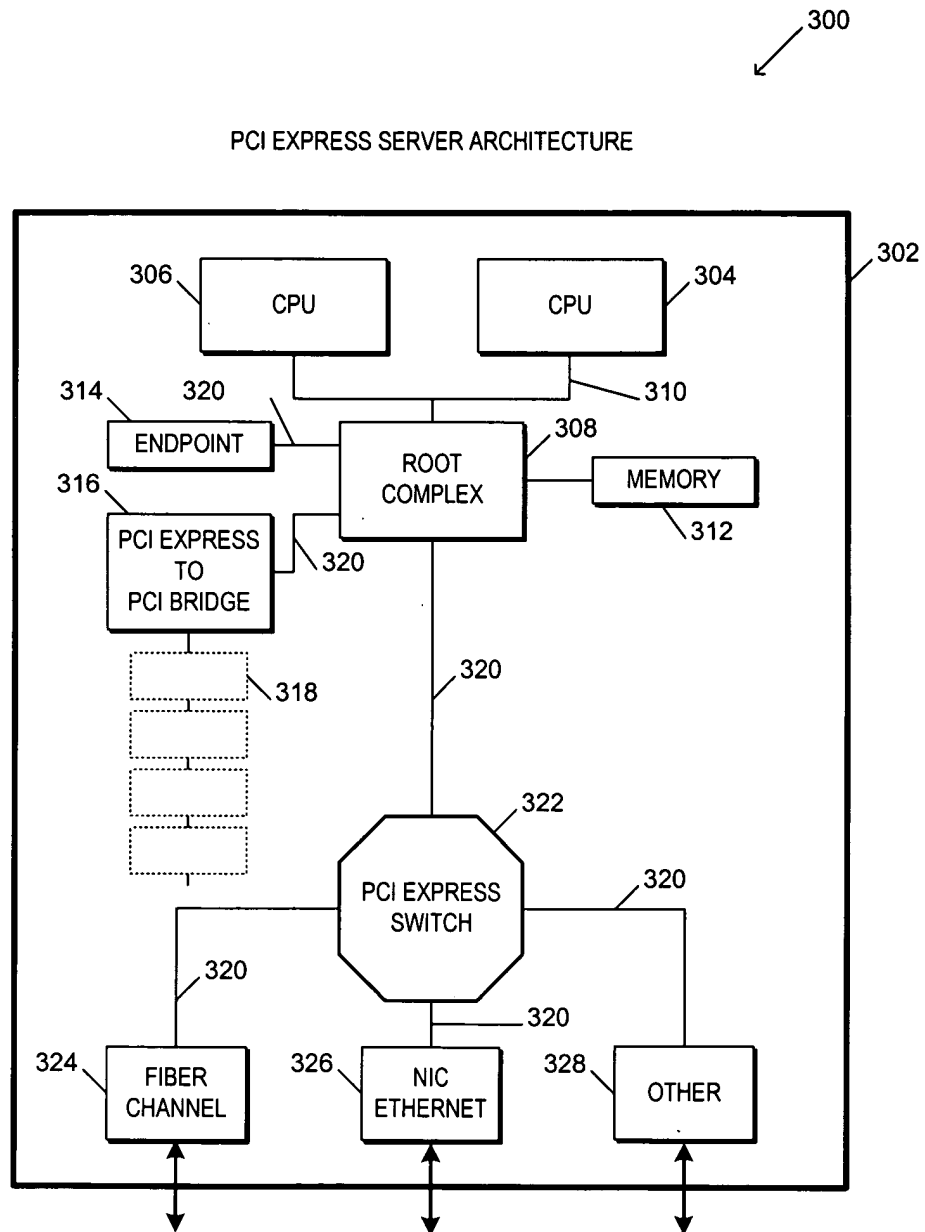


FIG. 4

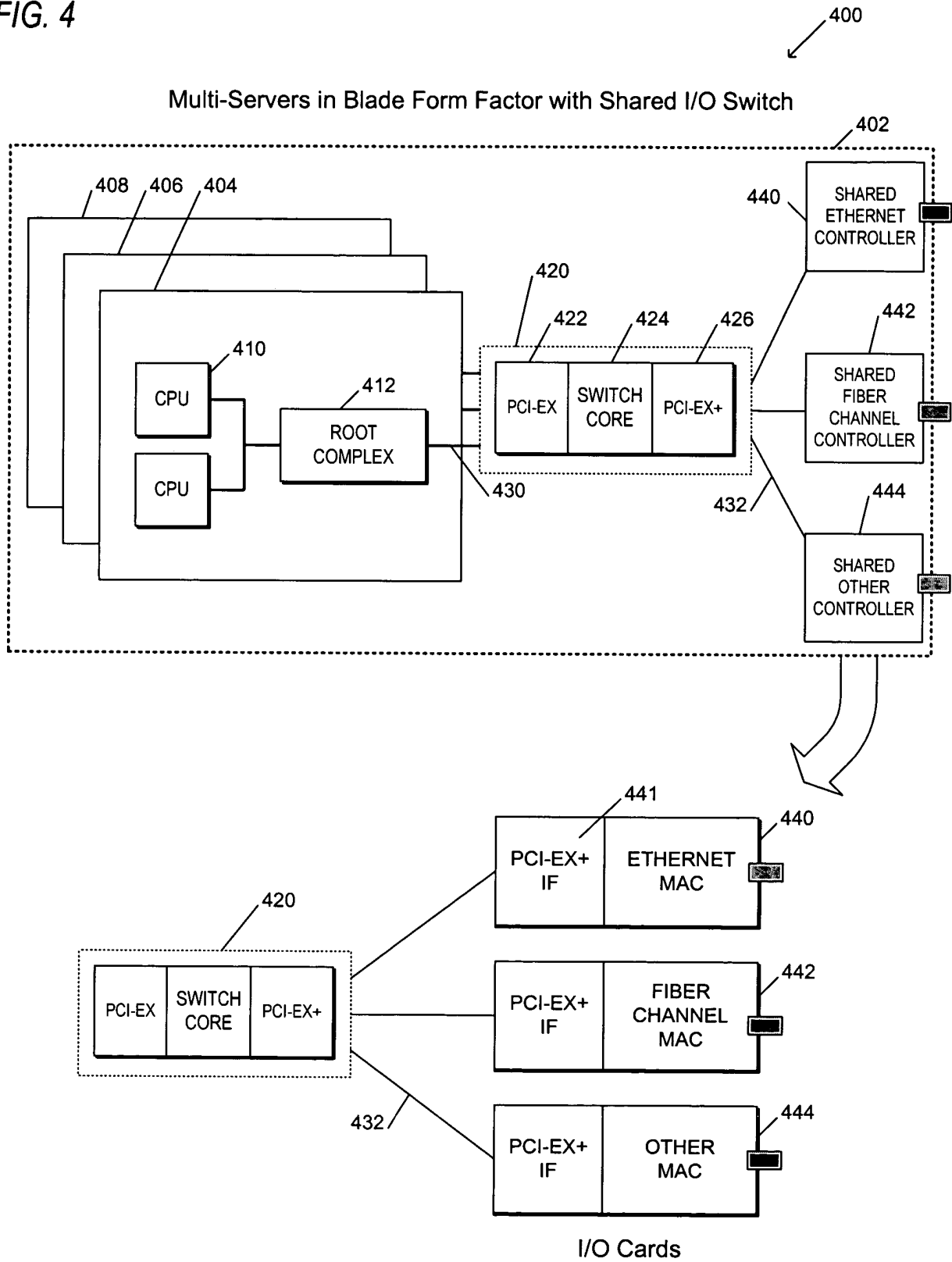


FIG. 5

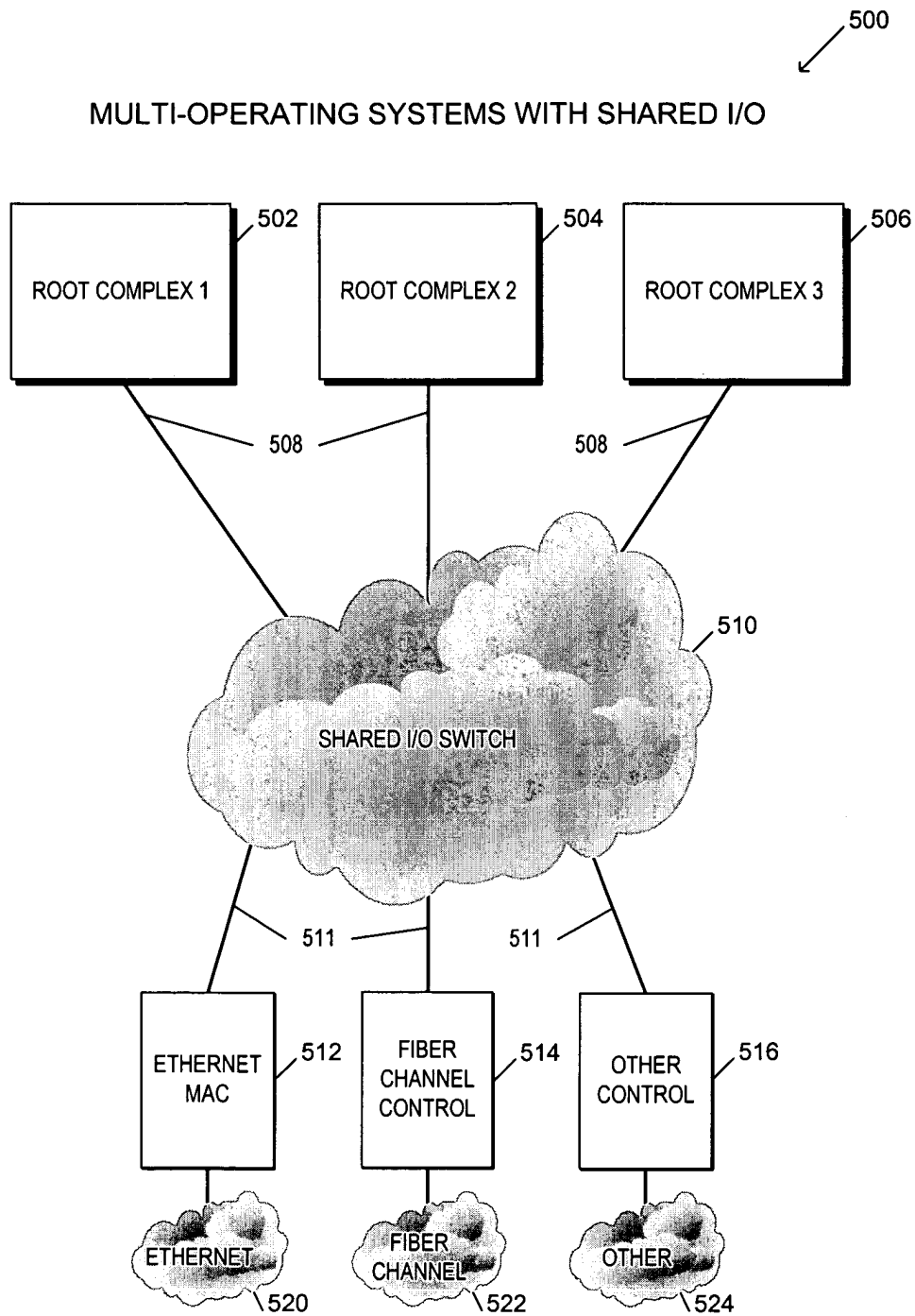


FIG. 6

MULTI-OPERATING SYSTEMS WITH SHARED ETHERNET CONTROLLER

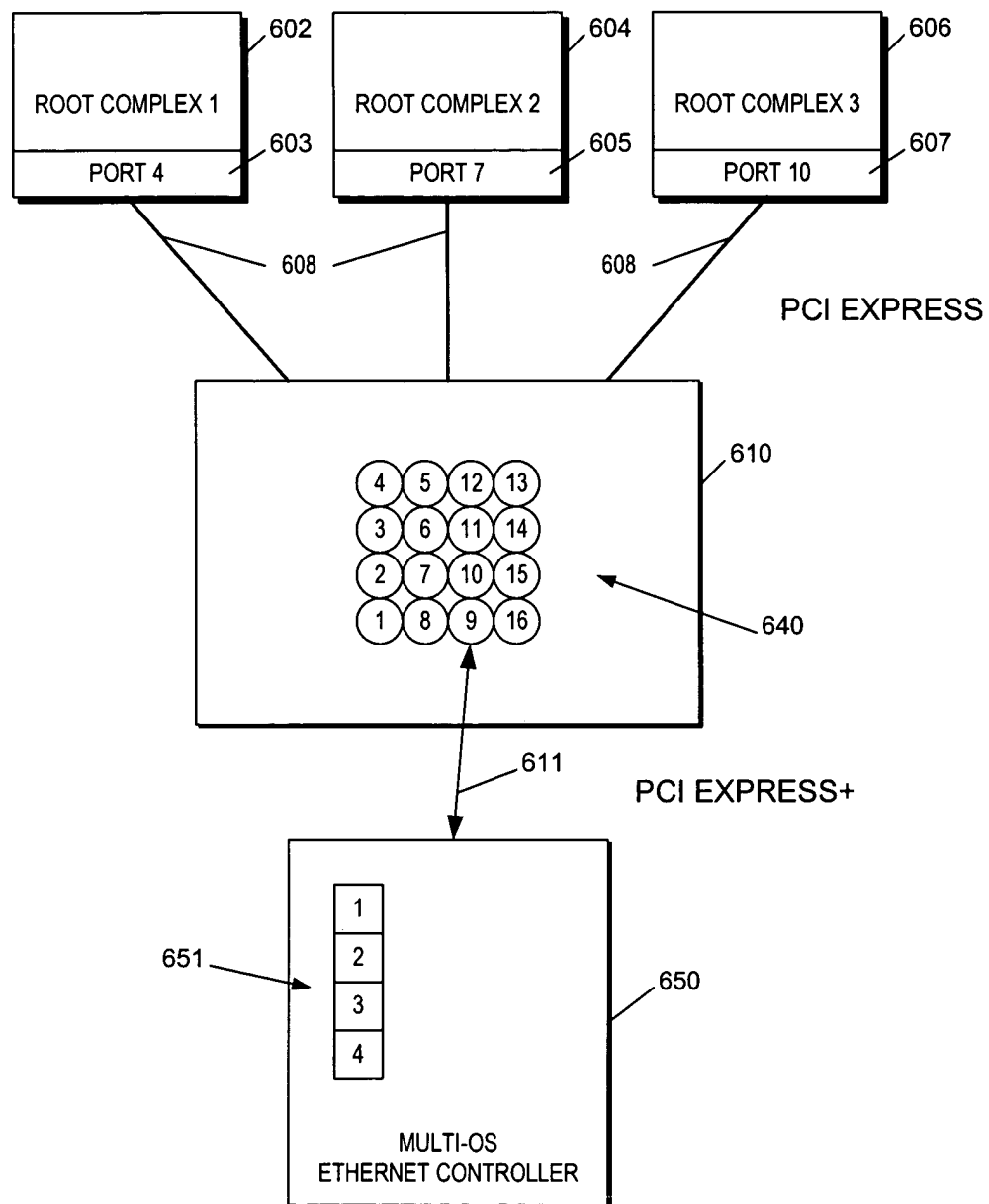


FIG. 7

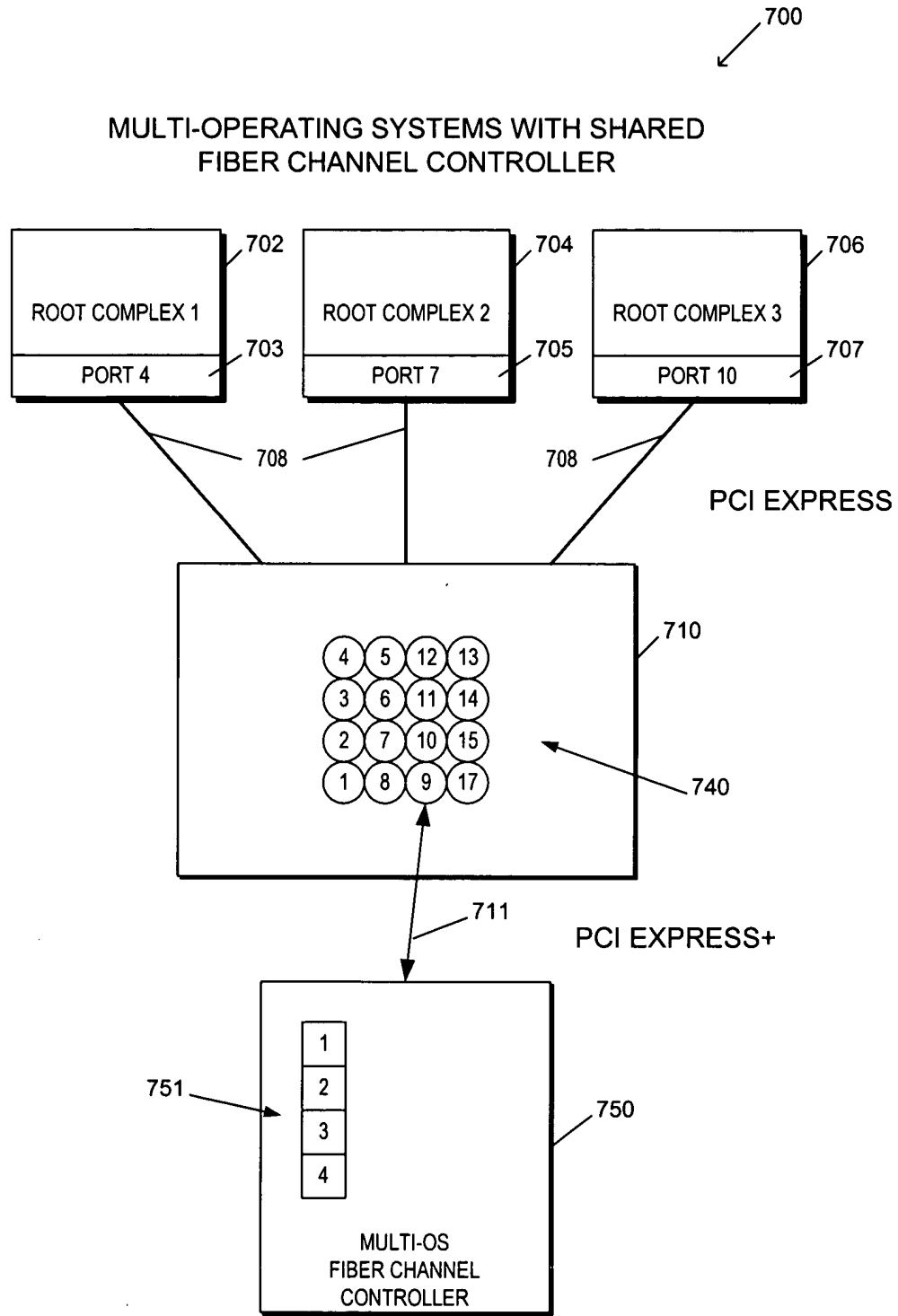


FIG. 8

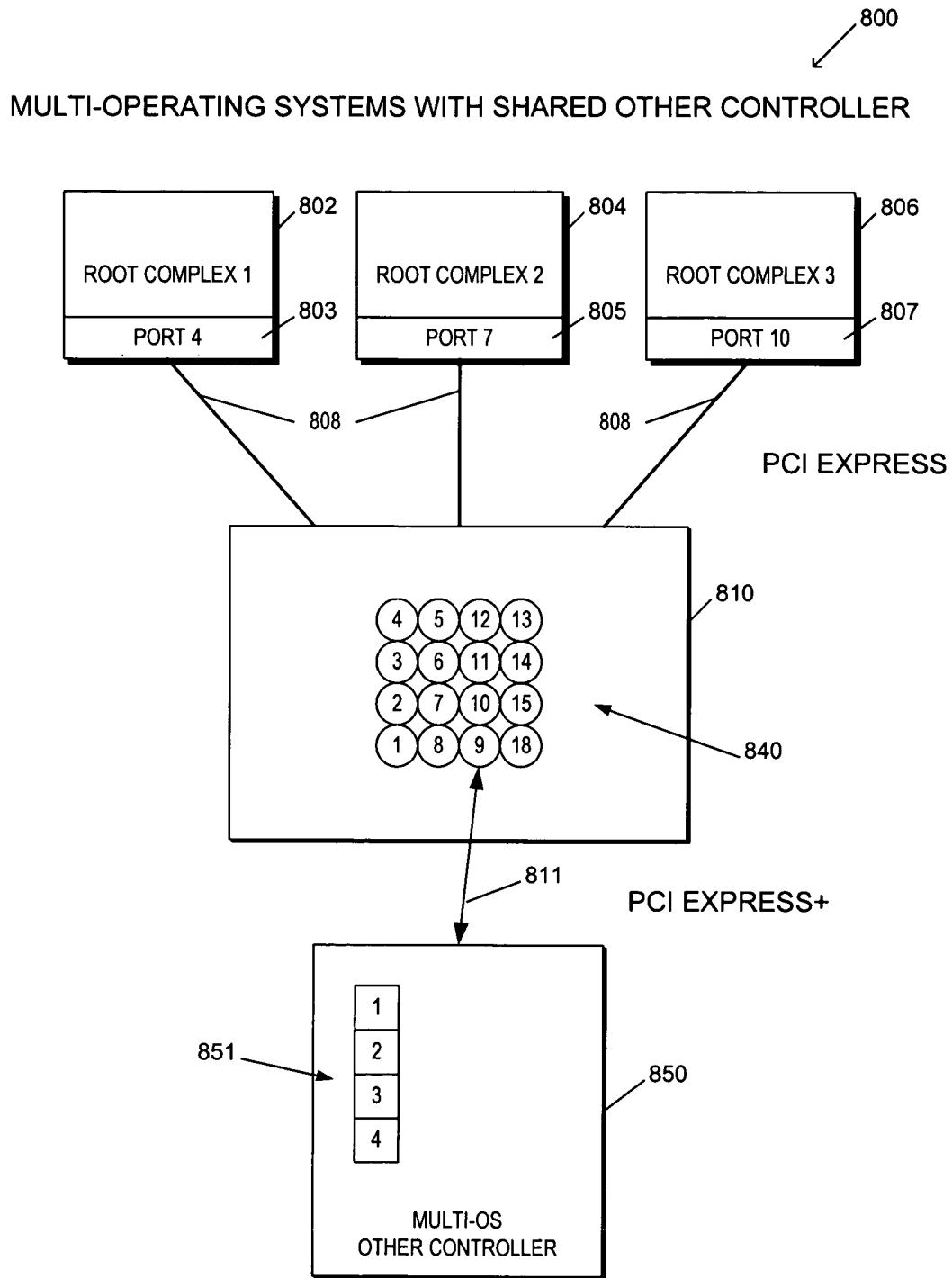


FIG. 9

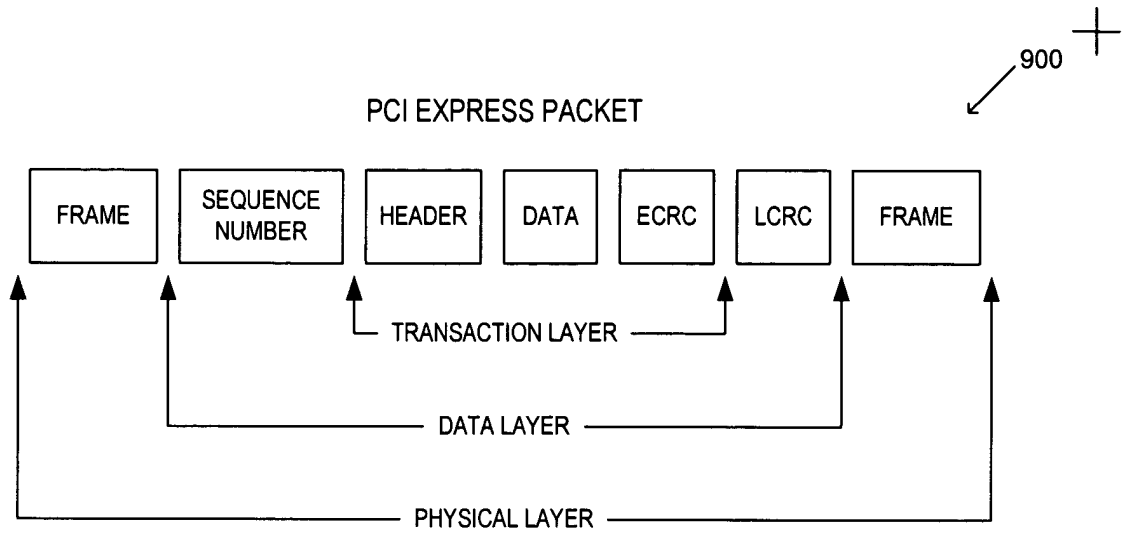


FIG. 10

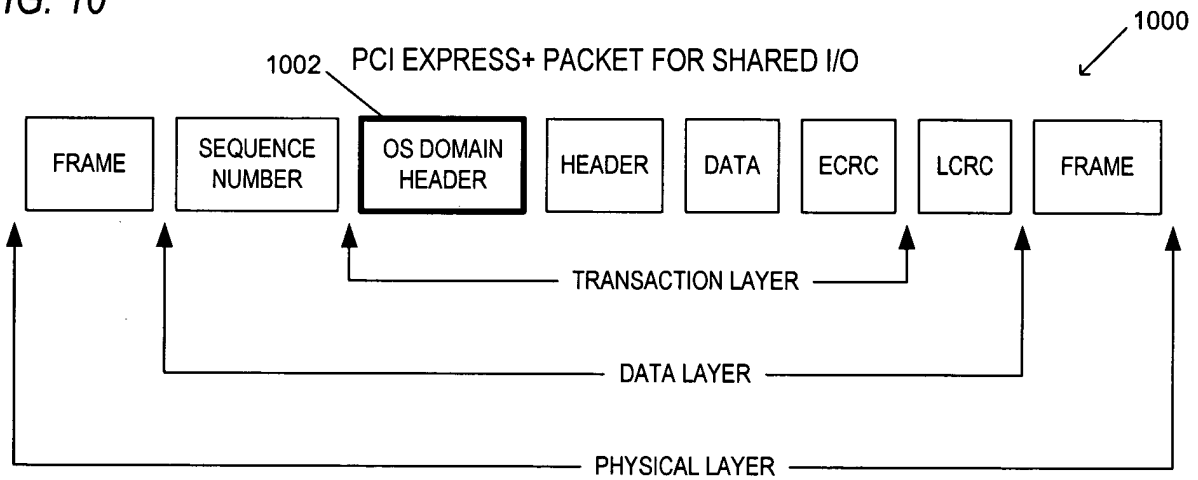
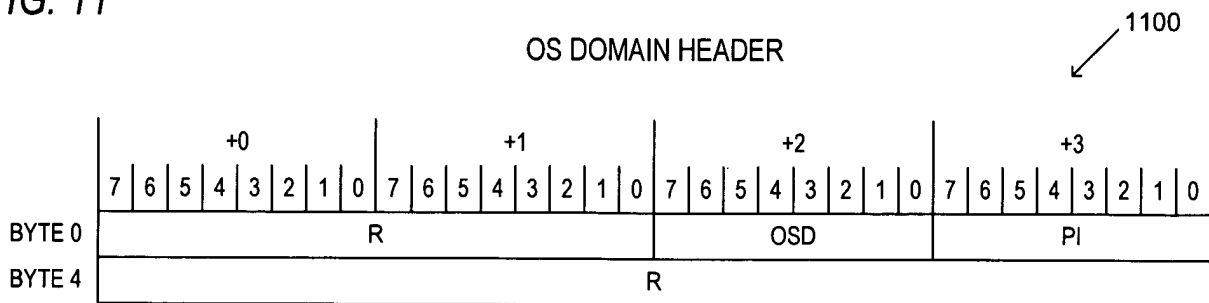


FIG. 11



PI Protocol ID Field
 OSD OS Domain Number
 R Reserved

FIG. 12 (Prior Art)

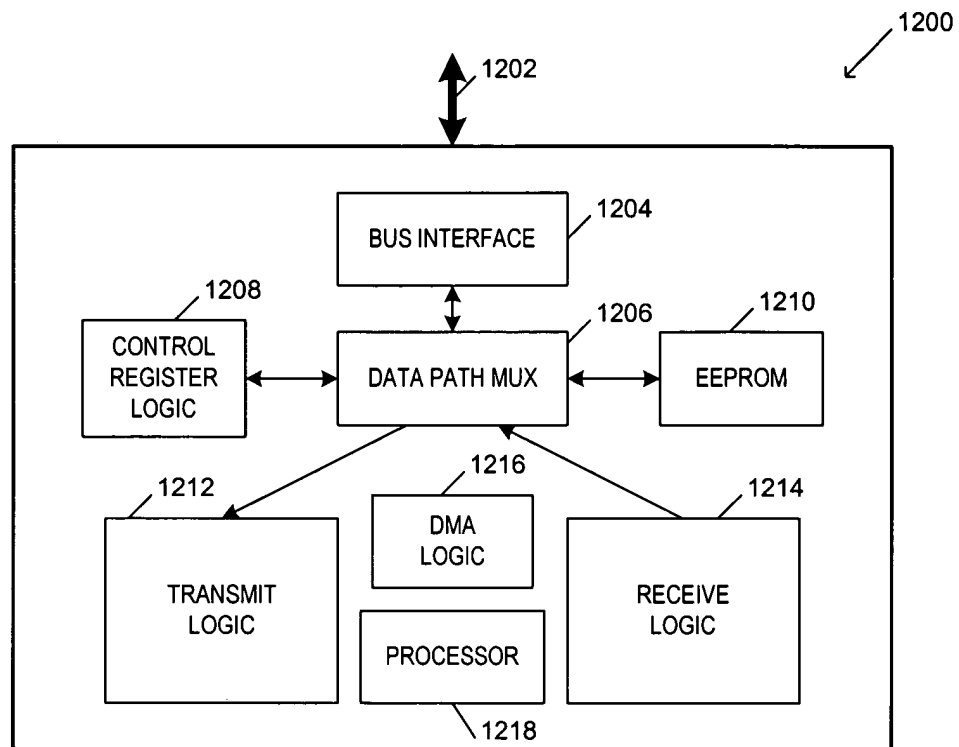


FIG. 13

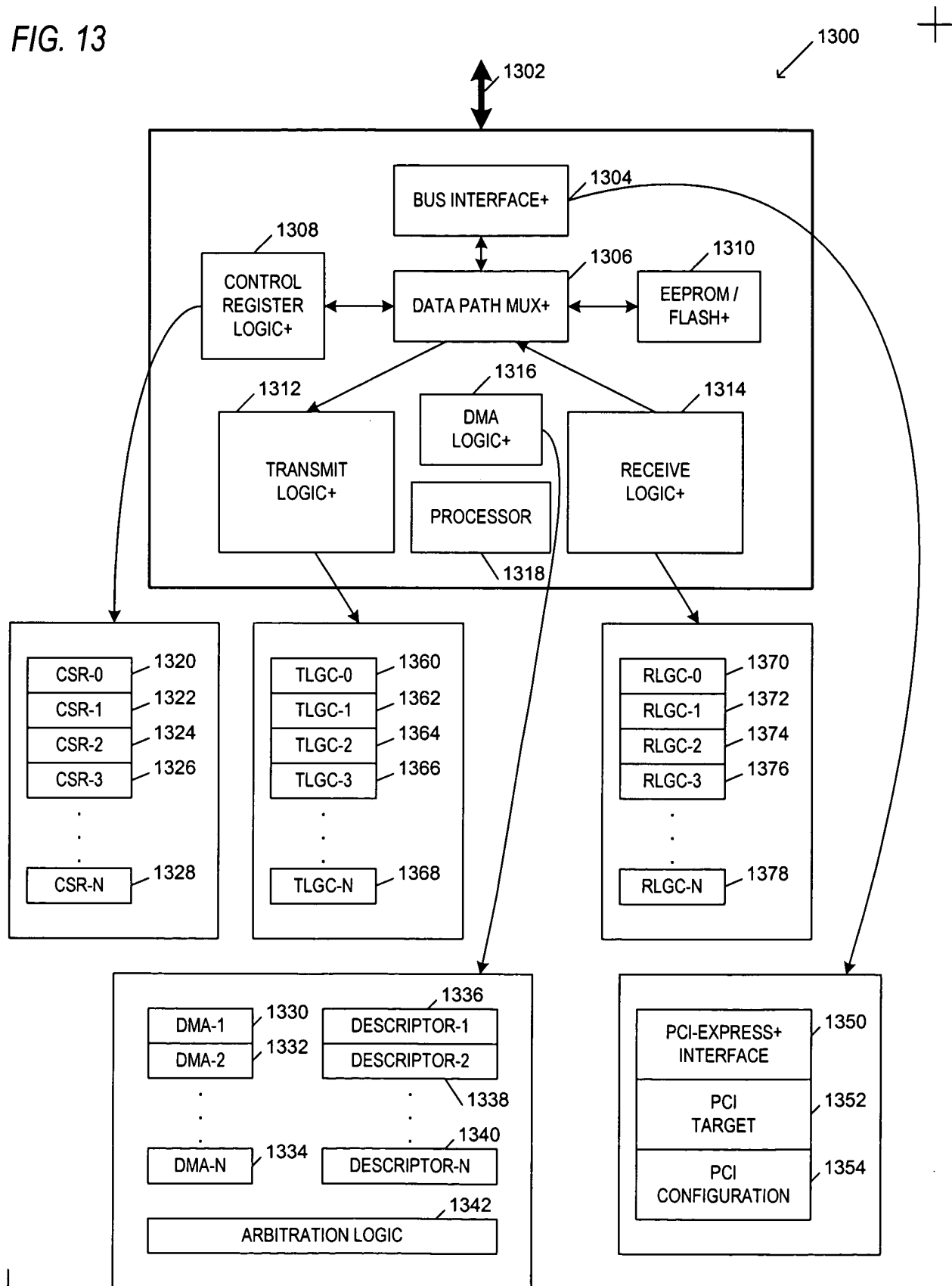


FIG. 14

MULTI-OPERATING SYSTEMS WITH SHARED ETHERNET CONTROLLER
PACKET FLOW EXAMPLE

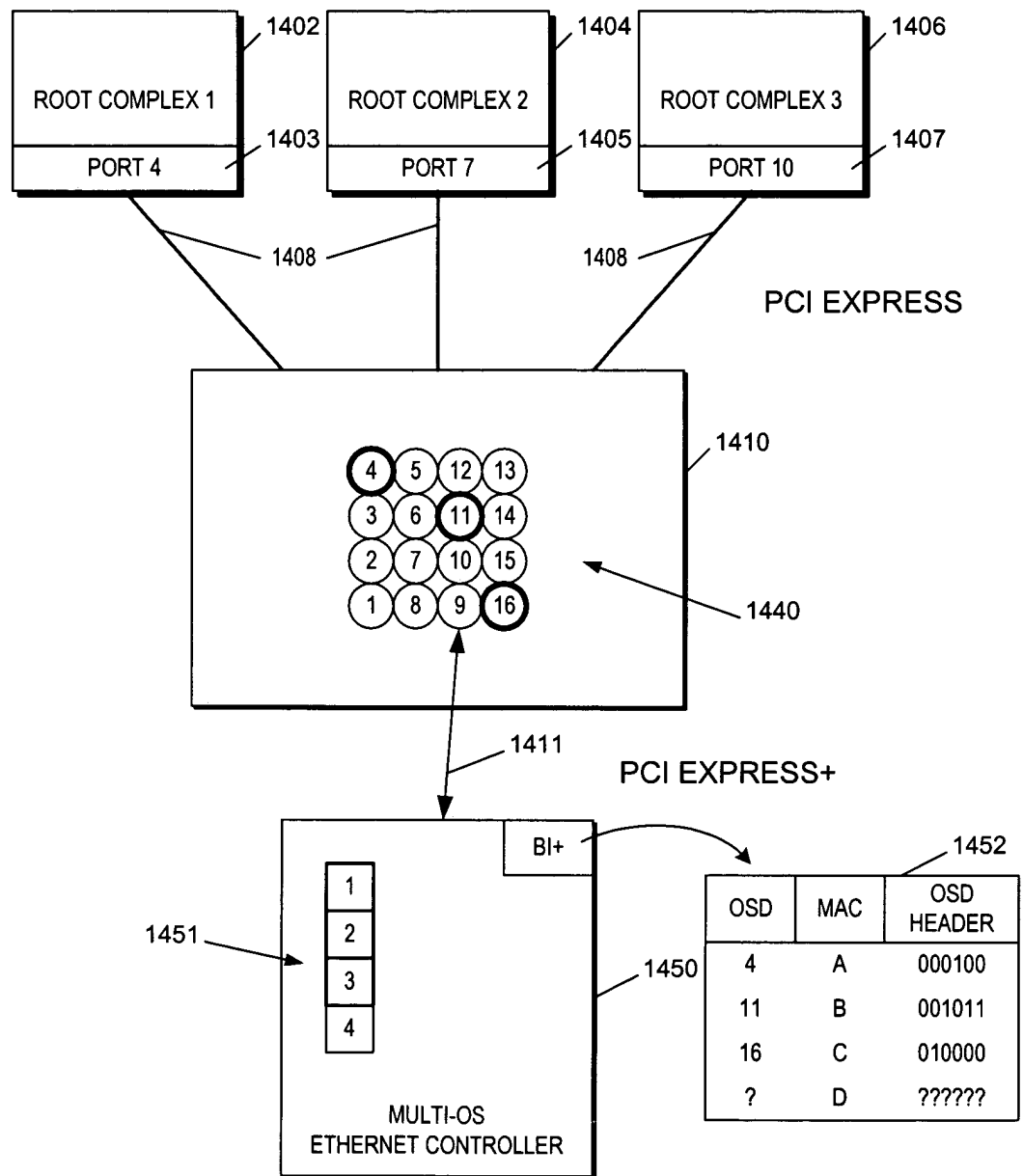


FIG. 15

METHOD OF SHARED I/O DOWNSTREAM TRANSMISSION FROM SWITCH

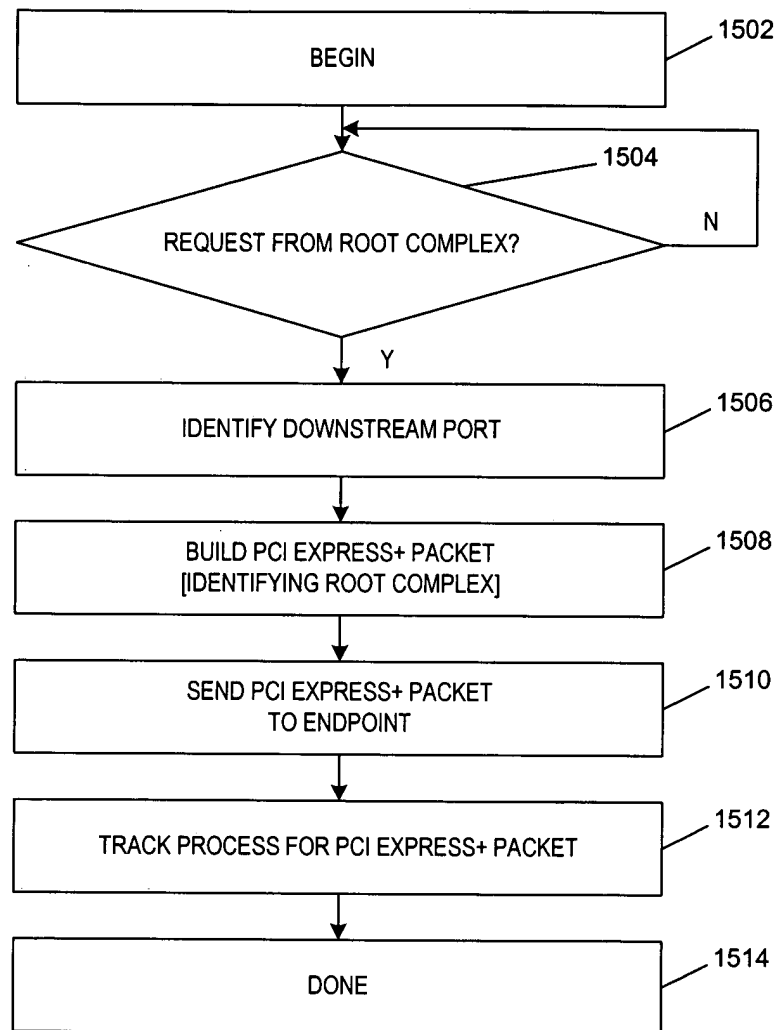


FIG. 16

METHOD OF SHARED I/O UPSTREAM TRANSMISSION TO SWITCH

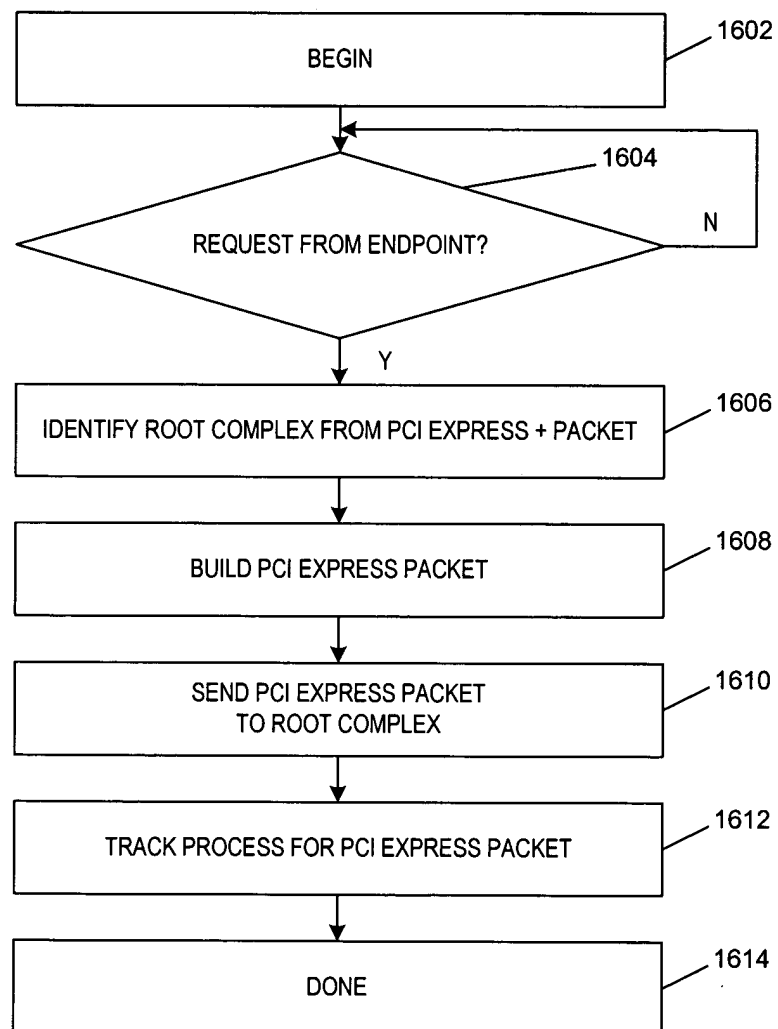


FIG. 17

METHOD OF SHARED I/O DOWNSTREAM TRANSMISSION TO ENDPOINT

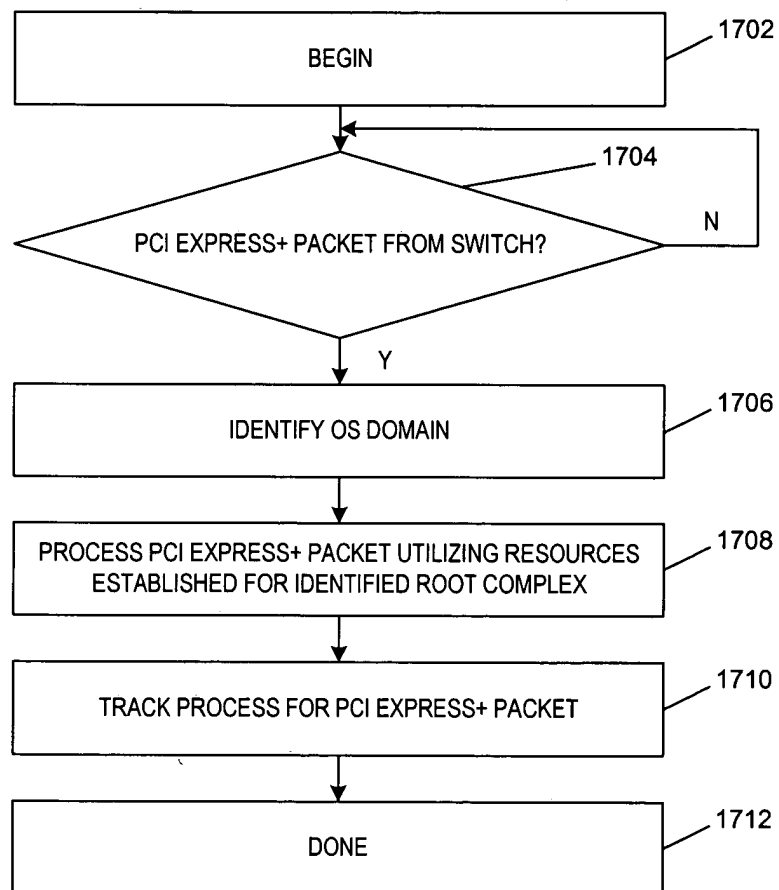


FIG. 18

METHOD OF SHARED I/O UPSTREAM TRANSMISSION FROM ENDPOINT

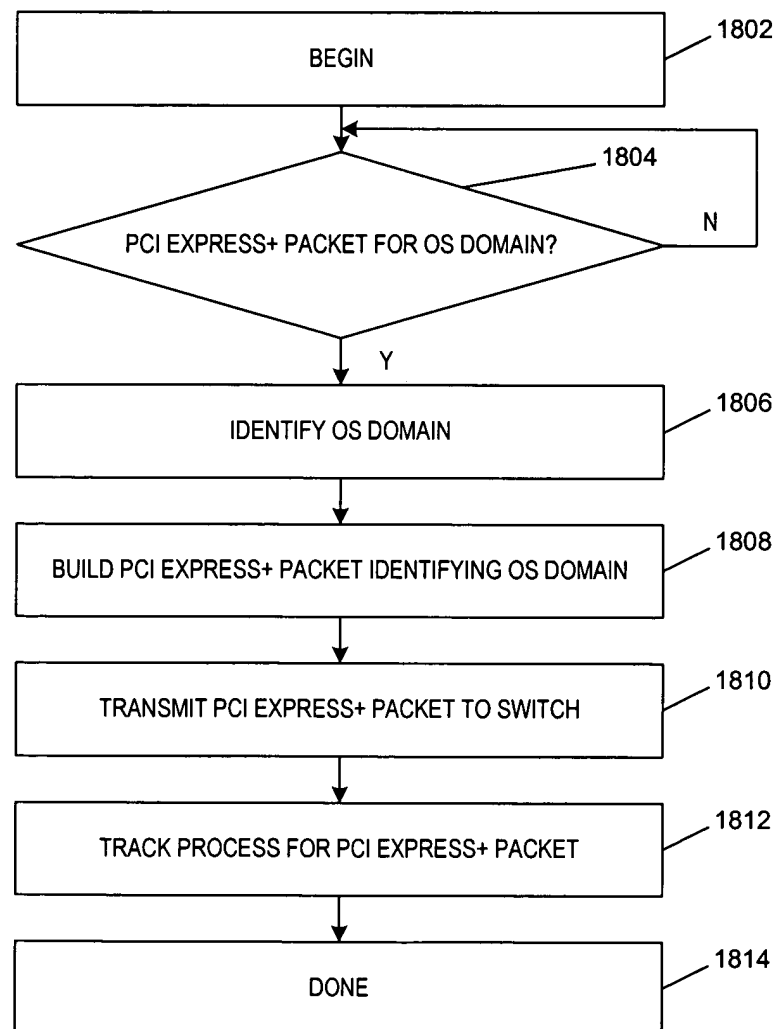
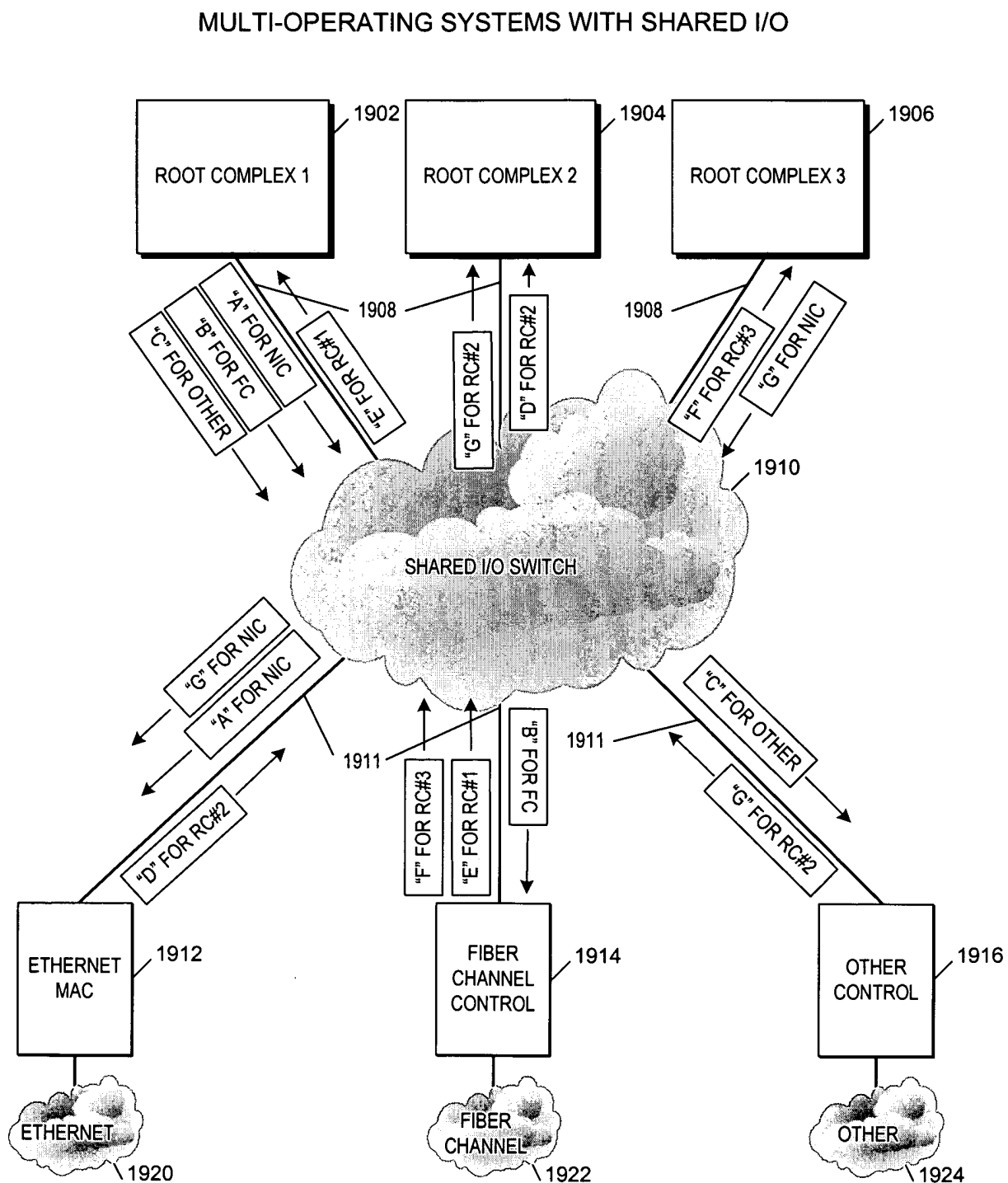


FIG. 19

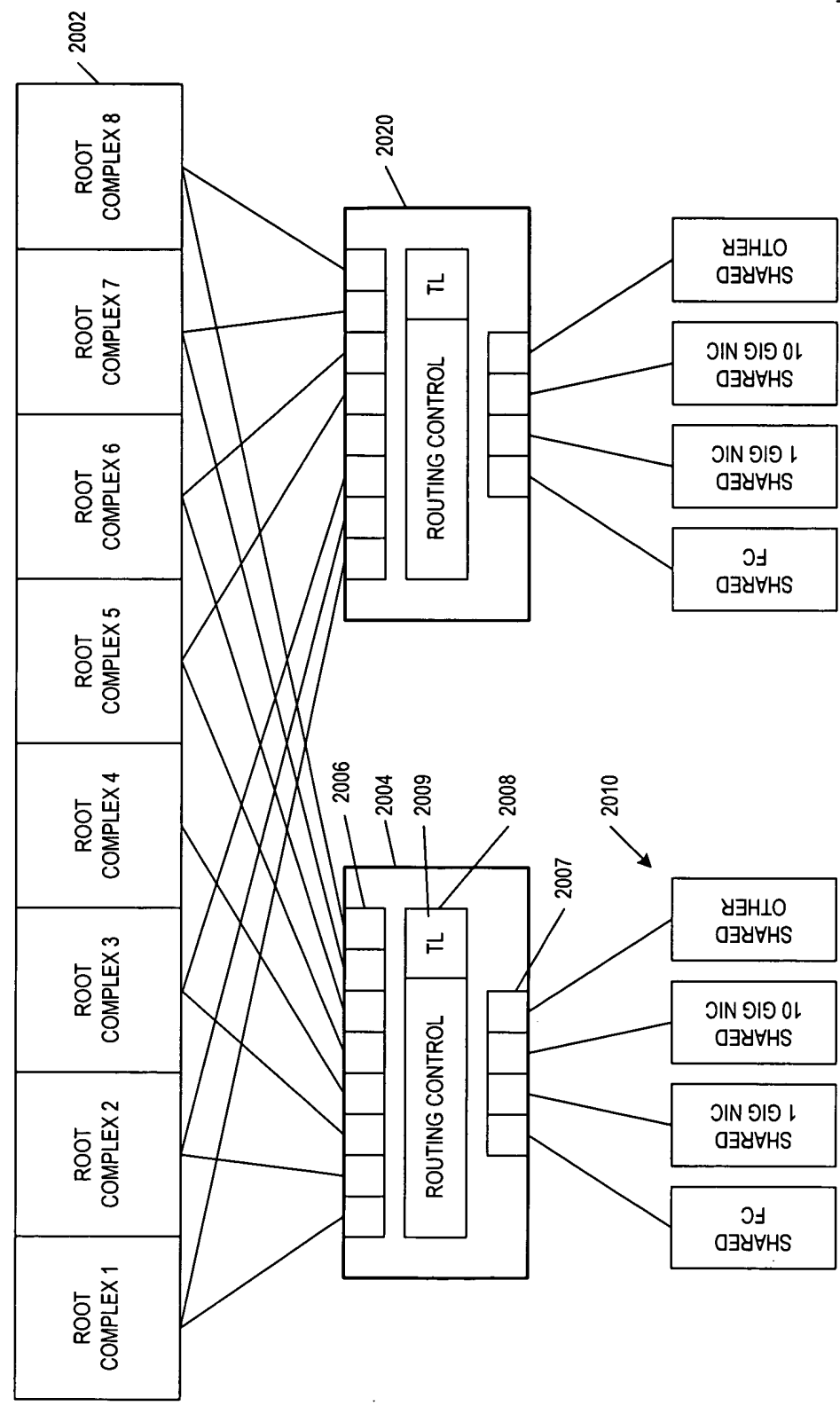


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FIG. 20

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8 BLADE REDUNDANT ARCHITECTURE WITH SHARED I/O SWITCHES AND ENDPOINTS



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